FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO. 0077.20 (1778.0120002)	APPLICATION NO. 09/364,786
APPLICANT Thekkath *et al.*	
FILING DATE July 30, 1999	GROUP 2672

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
Dᘔᒪ	AA1	5,619,198	04/1997	Blackham *et al.*			
Dᘔᒪ	AB1	6,175,907	01/2001	Elliott *et al.*			
	AC1						
	AD1						
	AE1						
	AF1						
	AG1						
	AH1						
	AI1						
	AJ1						
	AK1						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL1						Yes No
	AM1						Yes No
	AN1						Yes No
	AO1						Yes No
	AP1						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

Dᘔᒪ	AR	1	*MIPS IV Instruction Set (R10000)*, Revision 3.2, MIPS Technologies, Inc., entire publication submitted (September, 1995).
Dᘔᒪ	AS	1	*MIPS RISC Architecture - Volume I - Introduction to the ISA*, MIPS Technologies, Inc., entire publication submitted (August, 1998).
Dᘊ	AT	1	*MIPS RISC Architecture - Volume II - The Instruction Set*, MIPS Technologies, Inc., entire publication submitted (August, 1998).

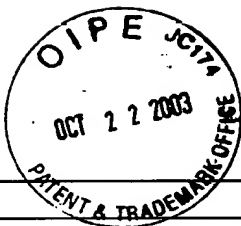| EXAMINER Daniel chuy	DATE CONSIDERED 2/1/07

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	AA2						
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL2						Yes No
	AM2						Yes No
	AN2						Yes No
	AO2						Yes No
	AP2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

DTC	AR	2	Kubosawa, H. et al., "Four-way VLIW Geometry Processor for 3D Graphics Applications," FUJITSU Sci. Tech. J., 36, 1, pp.39-47 (June 2000) (manuscript received December 1, 1999).
DTC	AS	2	Thekkath et al., "An Architecture Extension for Efficient Geometry Processing," slides 1-23, presented at Hot Chips 11, A Symposium of High-Performance Chips, Stanford Univ. (August 1999) (submitted for conference review July 14, 1999).
DTC	AT	2	Uhler, M., "Optimizing Game Applications for the MIPS RISC Architecture," Computer Game Developer's Conference, San Jose, CA, 14 pages (March 1999) (submitted for conference review on 2/12/99).

EXAMINER Danrl Chung	DATE CONSIDERED 2/7/0)

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	AA3						
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	AL3						Yes No
	AM3						Yes No
	AN3						Yes No
	AO3						Yes No
	AP3						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

DℸC	AR	3	Uhler, M., "Optimizing Game Applications for the MIPS RISC Architecture," *Computer Game Developer's Conference*, San Jose, CA, slides 1-22 (March 1999).
DℸC	AS	3	*AltiVec™ Technology Fact Sheet*, Motorola, Inc., 2 pages (1998).
DℸC	AT	3	*AltiVec™ Technology Programming Environments Manual*, Rev. 0.1, Motorola, Inc., entire document submitted (November 1998).

EXAMINER David Chug	DATE CONSIDERED 2/11/03

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA4						
	AB4						
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL4						Yes No
	AM4						Yes No
	AN4						Yes No
	AO4						Yes No
	AP4						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

DZC	AR	4	*AltiVec™ Technology Programming Interface Manual*, Rev. 0, Motorola, Inc., entire document submitted (June 1999).
DZC	AS	4	Fuller, S., "Motorola's AltiVec™ Technology" [white paper], Motorola, Inc., 4 pages (1998).
DZC	AT	4	Diefendorff *et al.*, "AltiVec Extension to PowerPC Accelerates Media Processing," *IEEE Micro*, pp. 85-95 (March/April 2000).

EXAMINER Daniel Chung	DATE CONSIDERED 2/7/07

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	AA5						
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	AL5						Yes No
	AM5						Yes No
	AN5						Yes No
	AO5						Yes No
	AP5						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

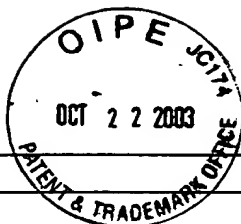|			
D?(	AR	5	*AltiVec™ Technology Programming Environments Manual*, Preliminary Rev. 0.2, Motorola, Inc., pp. i-viii, xi-xviii, 1-1 thru 1-11, 4-16 thru 4-33, 6-82, 6-122, 6-135, and 6-143 (May 1998)
D?(	AS	5	*3DNow!™ Technology Manual*, Advanced Micro Devices, Inc., entire document submitted (72 pages total) (May 1998).
b?(	AT	5	Copy of Office Action from U.S. Patent Application No. 09/249,177, filed February 12, 1999, 10 pages, mailed June 21, 2000.

EXAMINER Dayle Chuy	DATE CONSIDERED 1/9/03

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	AA6						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL6						Yes No
	AM6						Yes No
	AN6						Yes No
	AO6						Yes No
	AP6						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

DJC	AR	6	Rice *et al.*, "Multiprecision division on an 8-bit processor," Computer Arithmetic, 1997, Proceedings, 13th IEEE Symposium on 6-9 July 1997, pp. 74-81.
	AS	6	
	AT	6	

EXAMINER Daniel J Chuy	DATE CONSIDERED 8/7/03

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